Design and simulation of Differential Transimpedance Amplifier (TIA) Based on 0.18 µm CMOS Technology

Dr. Luqman Safar
Department of Electrical Engineering
University of Mosul

Muna Samir Zaki
Department of Electrical Engineering
University **of Mosul**

Abstract

The transimpedance amplifier is realized in a 0.18µm CMOS technology. The TIA uses a shunt-shunt feedback topology, differential TIA because it reaches a higher bandwidth than a conventional one. The TIA also has a variable gain to increase the bandwidth of the amplifier . The TIA has a maximum gain of 73 dBΩ, bandwidth 3.1GHZ, bit rate 5Gb/s and input-referred current noise of 5 pA/√Hz. Eye jitter at bit rate 5Gb/s equal to 5ps (peak to peak).

Keywords*:* transimpedance amplifier (TIA) , Berkeley Short Channel Igfet model (BSIM model) , Advanced design system (ADS) .

تصميم ومحاكاة مكبر الممانعة التفاضلية المبنية على تقنية 0.18 µm CMOS

د. لقمان سفر علي
قسم الهندسة الكهربائية
جامعة الموصل

منى سمير زكي
قسم الهندسة الكهربائية
جامعة الموصل

الخلاصة

مكبر الممانعة نفذ باستخدام تقنية 0.18 µm CMOS . واستخدم في هذا المكبر تغذية خلفية نوع توازي-توازي ،وتمت الاستعانة بمكبر الممانعة التفاضلية لان عرض الحزمة فيه اعلى مما هو في التقليدي ، كما ان المكبر ذو كسب متغير لزيادة عرض حزمة التردد للمكبر .حيث بلغ اعلى كسب للمكبر 73 dBΩ وبعرض حزمة ترددية 3.1 GHZ وبمعدل نقل بيانات 5 Gb/s ، وضوضاء تيار الادخال 5pA/√HZ . وبلغ الانحراف الزمني (jitter) 5 ps (peak to peak) عند معدل نقل بيانات 5 Gb/s .

Received: 3– 1 - 2012 **Accepted: 3 – 10 - 2012**

Introduction:

In an optical communication system, optoelectronic receiver, which consists of a photo detector and a trans impedance amplifier, is used to convert the optical signals into electrical signals in the front end. Figure (1) shows the system block diagram of optical fiber communication [1]. A tele- and data-communications are developed rapidly. Optic-fiber networks are widely implemented and the data speeds of the systems get higher and higher. Accordingly, ultra-high speed ICs for different systems is needed. Up to now, however, most ICs at gigabit per second are manufactured in GaAs and bipolar Silicon technologies at higher cost. As the feature size getting smaller, CMOS technologies begin to take an important role in high performance and high speed ICs. Nowadays, a feature size of 0.35-, 0.25-, and 0.18-μm CMOS technologies are available. The simulated unity current gain cut off frequency (f_T) of the above sub-micron CMOS technologies are 13.5-, 18.6-, and 49-GHz، respectively. Conservatively, a transistor can be operated at the frequency of $f_T/10$. Thus, these submicron CMOS technologies can be used in the ICs with upper frequencies of 1.35-, 1.86-, and 4.9-GHz, respectively. Further, 1-Hz frequency band can carries approximately 2 bit data, resulting in the highest bit rates of >2.5-, >3.5-, and ≈10 Gb/s for three sub-micron CMOS technologies [2] .

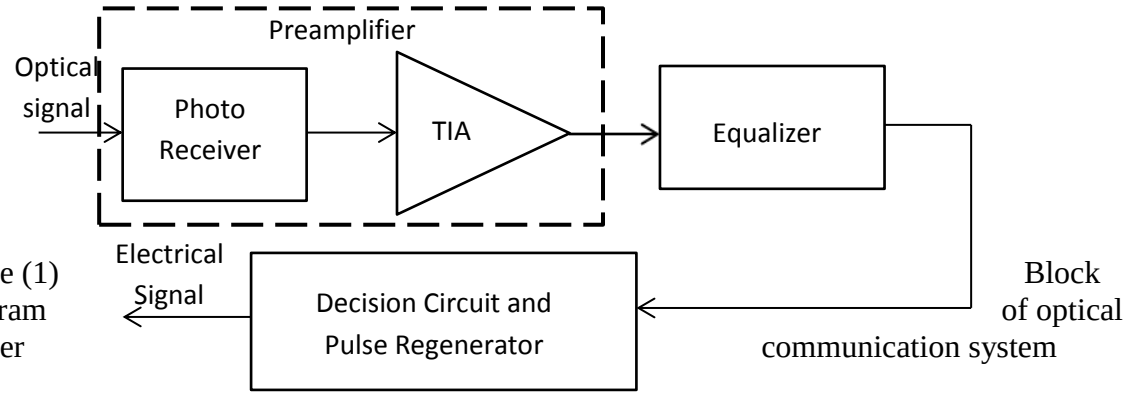


Figure (1) diagram fiber

Out of the four amplifier types, namely voltage, trans impedance, trans conductance, and current amplifiers [3]. In this work, a CMOS variable-gain fully differential trans impedance feedback amplifier is presented.

Circuit Topology:

The trans impedance amplifier converts the current generated by the photodiode into an output voltage [4]. The design of this circuit involves many trade-offs between noise, bandwidth, gain, chip area and power dissipation. The simple topology of feedback trans impedance amplifier shown in figure (2), Since $V_{in} = V_{out}/-A$, where V_{in} , V_{out} are the input and output voltages of amplifier respectively and A the open loop voltage gain of core amplifier, we have:

$$\frac{V_{out}/A}{R_{FB}} = -I_{in} - \left(\frac{Vout}{A}\right) C_{PD} s \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

That is,

$$\frac{V_{out}}{I_{in}} = Z_T = -\frac{A}{1+A}\ \frac{R_{FB}}{1+\frac{R_{FB}C_{PD}}{1+A}s} \qquad \ldots\ldots\ldots\ldots (2)$$

Where $I_{in}$the input current of amplifier, C_{PD} is the capacitance of the photodiode, R_{FB} is the feedback resistance and Z_T is the transimpedance gain. At low frequencies the transimpedance gain and equal to :

$$Z_T = -\frac{A}{1+A}R_{FB} \qquad \ldots\ldots\ldots (3)$$

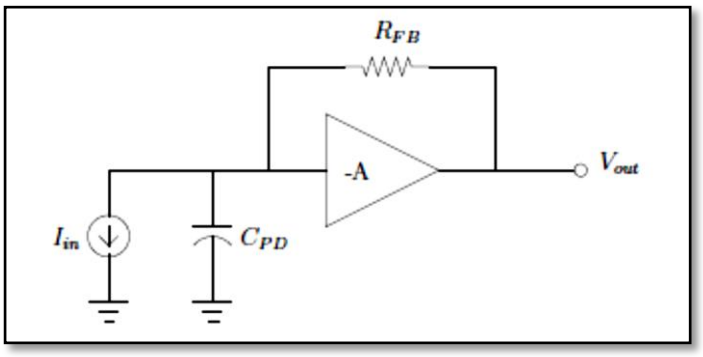


Figure (2) feedback Trans impedance amplifier

Figure (3) shows a schematic of the typical single-ended CMOS trans impedance preamplifier. The amplifier consists of a common-source stage and a source follower. The source follower isolates R_D from the loading effect of Both R_{FB} and the input capacitance of the subsequent stage. In our analysis, the channel-length modulation and body effect are neglected for simplicity. If the output impedance of the source follower ($1/g_{m2}$) ,is much less than R_{FB}, the open loop voltage gain of the amplifier is approximately equal to $g_{m1}R_D$ and the closed loop trans impedance gain is

$$Z_T = \frac{g_{m1}R_D}{1+g_{m1}R_D}R_{FB} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Where g_{m1}, g_{m1} are the trans conductance of M_1 and M_2 respectively.

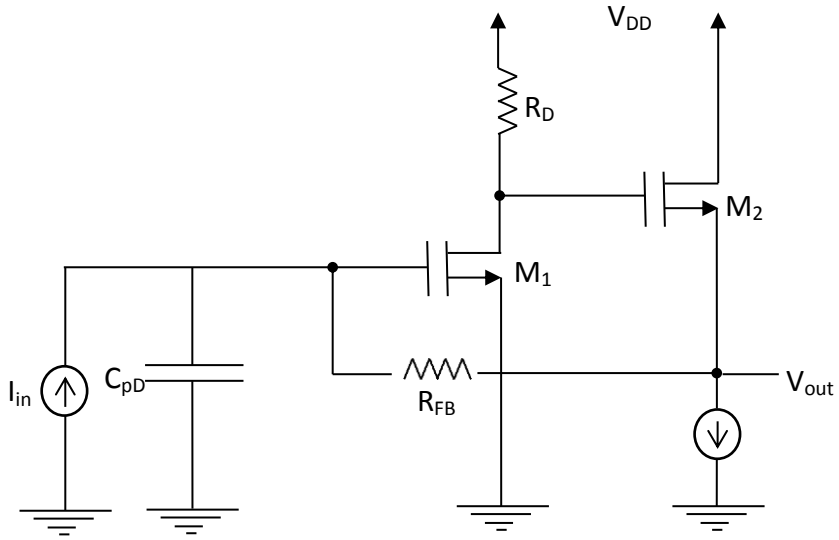


Figure (3) single-ended CMOS feedback trans impedance amplifier

From the principle of feedback system [4], the input of the feedback amplifier equal to:

$$R_{in} \approx \frac{R_{FB}}{1+A} \approx \frac{R_{FB}}{1+g_{m1}R_D} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

And output impedances at low frequencies is given by:

$$R_{out} \approx \frac{r_{dg2}}{1+A} \approx \frac{1/g_{m2}}{1+g_{m1}R_D} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

To compute the input-referred noise current of theTIA using the topology of Figure (4). Viewing M_1,R_D,and M_2 as the core voltage amplifier and neglegting channal length modulation and body, the output noise voltage as :

$$\overline{V_{n,out,core}^2} = 4kTg_{m1}\gamma R_D^2 + 4kTR_D + 4kT\frac{\gamma}{g_{m2}} \quad \ldots\ldots\ldots\ldots\ldots (7)$$

Where

γ denotes the excess noise coefficient, equal to 2/3 for long channel devices and reaching as high as 2.5 in deep submicron technologies [5].

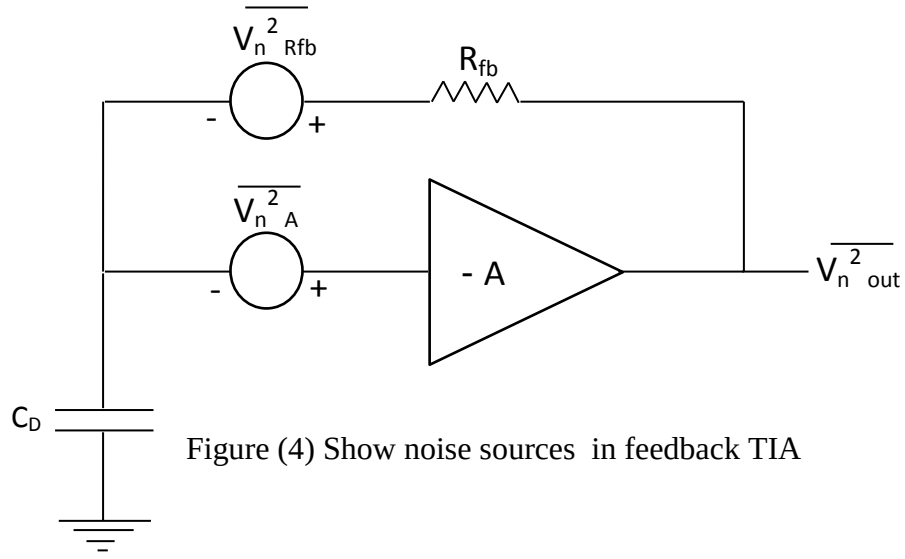


Figure (4) Show noise sources in feedback TIA

Where the last term represents the gate-referred noise voltage of M_2.Dividing equation (7) by the square of the voltage gain yields the input-referred noise of the core:

$$\overline{V_{n,in,core}^2} = 4kT\frac{\gamma}{g_{m1}} + \frac{4kT}{g_{m1}^2R_D} + 4kT\frac{\gamma}{g_{m2}g_{m1}^2R_D^2} \quad \ldots\ldots\ldots\ldots (8)$$

The input noise current is

$$\overline{I_{n,in}^2} = \frac{4kT}{R_{fb}} + \frac{\overline{V_{n,in,core}^2}}{R_{fb}^2} \quad \ldots\ldots\ldots\ldots (9)$$

$$\overline{I_{n,in}^2} = \frac{4kT}{R_{fb}} + \frac{4kT}{R_{fb}^2}\left(\frac{\gamma}{g_{m1}} + \frac{1}{g_{m1}^2} + \frac{\gamma}{g_{m2}g_{m1}^2R_D^2}\right) \quad \ldots\ldots\ldots\ldots\ldots (10)$$

For a given trans impedance gain, only the noise contributed by the core can be minimized. This requires maximizing R_D and the trans conductance of M_1 and M_2.

Circuit design:

- Differential trans impedance amplifier

The system presented in this paper is shown in Figure (5) using double balanced photo diode and three stage differential trans impedance amplifier .The differential trans impedance amplifier is chosen also because its complementary outputs of the trans impedance amplifier stage allows a differential interface to the following differential main amplifier stage, which is advantageous at high speed data rates. Another important advantage is that the differential configuration throughout the photo-receiver reduces the effect of bond wire inductance of ground and supply voltage by reducing simultaneous switching currents. This is important, since experience has shown that single-ended amplifiers have a tendency to common-mode oscillation [6]. The circuit is designed to operate at a bit-rate of 5-Gbit/s, while operating from a supply voltage of 3.5 V. Figure (6) shows the schematic of fully differential trans impedance amplifier, The first stage of the trans impedance amplifier is chosen to be a fully differential common source with shunt feedback resistance and a resistive load. Its basic function is to convert the input current into an output voltage, stage 2 is a buffer stage with two-source follower providing isolation between the input and output of the amplifier, The third stage is a fully differential output stage, This stage further increases the gain of the amplifier.

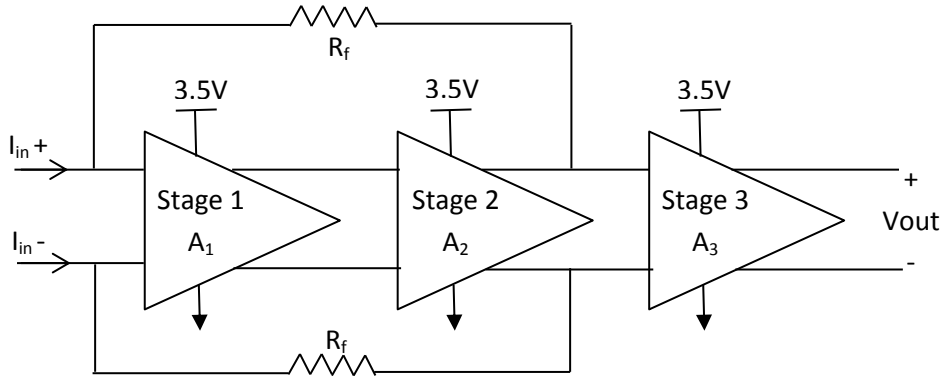


Figure (5) Circuit diagram of three stage trans impedance design with single power supply

- Variable Gain TIA

In order to avoid saturating the amplifier when the high amplitude signal is applied, the TIA is designed to have a variable gain. The gain, can be varied by adjusting the value of the feedback resistance, by placing a transistor PMOS type operating in the linear mode in parallel with the feedback resistor R_{fB} as shown in Figure (7). The drain of PMOS transistor connected to the input and source connected to the output. The bias voltage Vg is now for instance ground, when a signal is applied, the source voltage of the transistor increases, so any change in Vds is reflected in an equal change in Vgs and the transistor will stay in linear region, even for large signals, therefore PMOS transistor is chosen. In figure (7) when the gate voltage(Vg) of the transistor is increased, the transistor is turned on and begins to conduct, reducing the value of the total feedback resistance. On resistance of the transistor determines the tuning range. The overall feedback value R_f is given by:

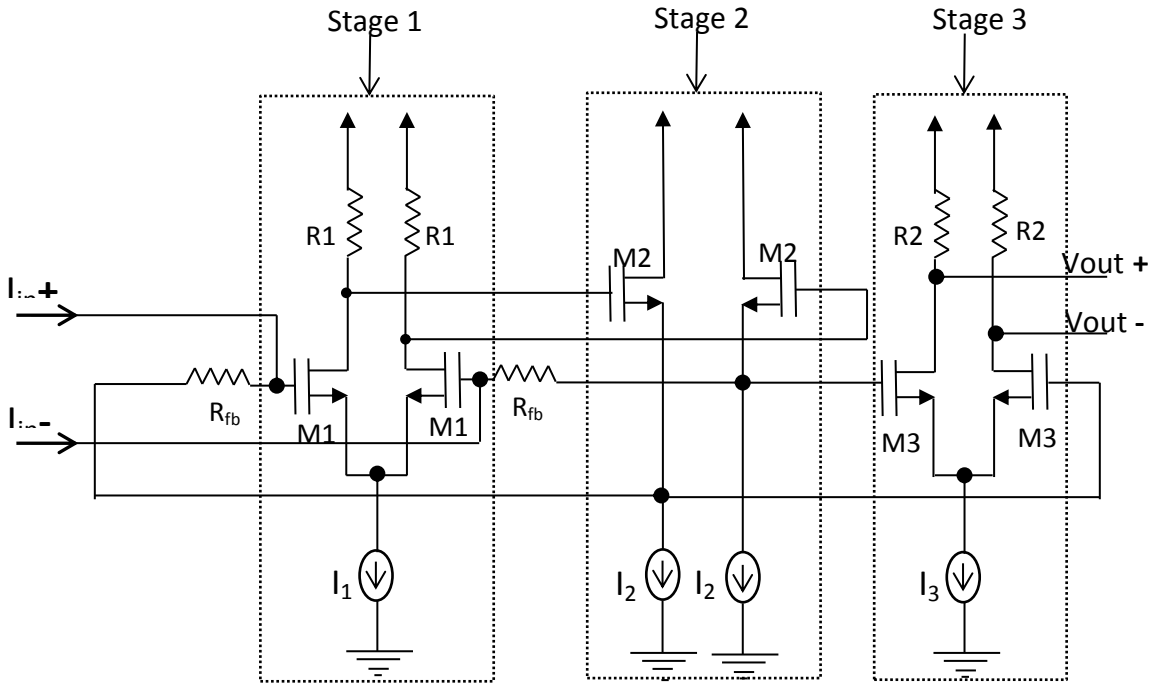


Figure (6) Differential transimpedance amplifier schematic

$$R_f = R_{fb} // R_{MRfb} \qquad \text{.....(11)}$$

$$R_{MRfb} \cong \frac{1}{\mu_p C_{ox} \left(\frac{W}{L}\right)_{MRfb} \left(|V_{gs}| - |V_T| - |V_{ds}|\right)} \qquad \text{.....(12)}$$

Where: μ_p mobility. C_{ox} is the oxide capacitance. V_T the threshold voltage. and, $\left(\frac{W}{L}\right)_{MRfb}$ the dimensions of the PMOS transistor.

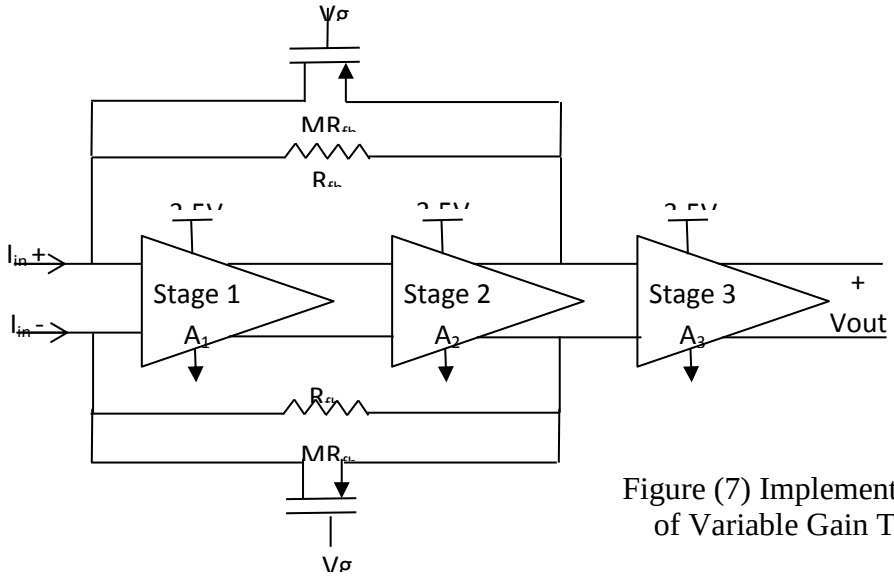


Figure (7) Implementation of Variable Gain TIA

Simulation Results:

The fully differential trans impedance amplifier has been simulated using BSIM 0.18 µm CMOS technology in ADS program. The frequency response of the closed-loop trans impedance feedback amplifier is shown in figure (8). Figure (8) (a) shows that the maximum trans impedance gain is 73dbΩ with bandwidth of 3.1 GHz and bit rate of 5Gbps. When Vg voltage increases the trans impedance amplifier gain will decrease and the bandwidth of the amplifier will increase as shown in figure(8) (b). This is because, as the Vg voltage increases, the total resistance of the feedback network will decrease. Figure (9) (a) shows simulated the average input referred noise current spectral density corresponding to the maximum gain is approximately 5 pA/√Hz, We can see in figure (9) (b) that as the Vg voltage is increased, the input referred noise current will increase.

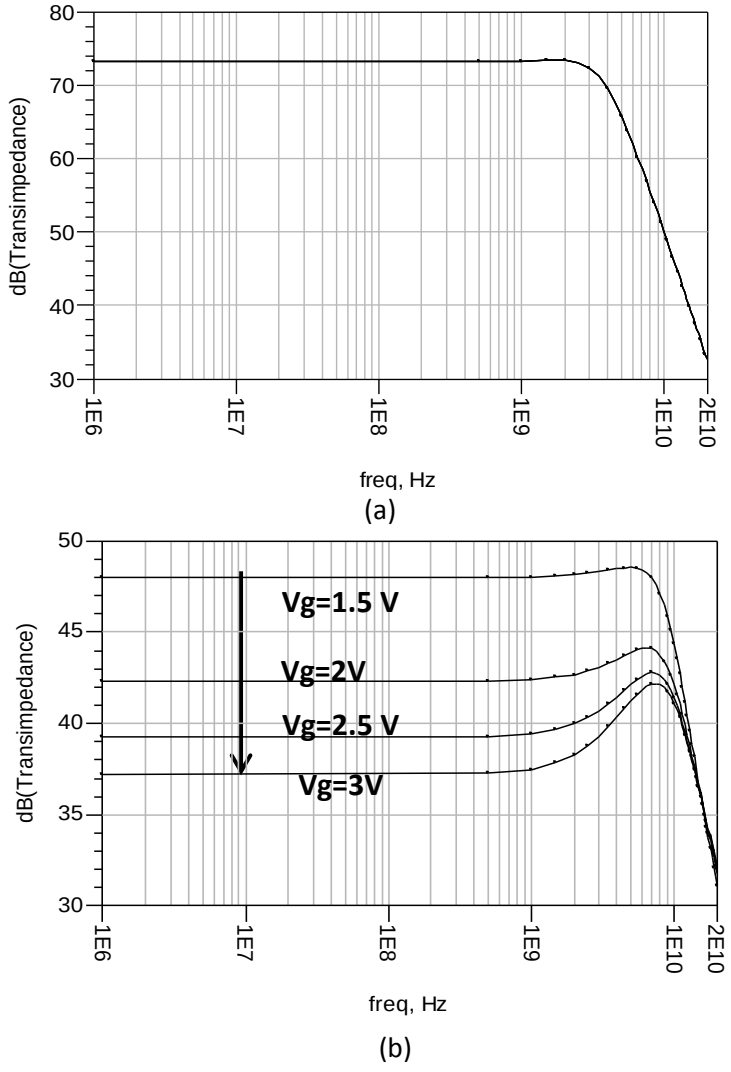


Figure (8) Trans impedance amplifier gain (a) without variable gain (b) with variable gain (Vg is varied from 1.5V to 3V step 0.5V)

This is because the transistor M_{Rfb} is now conducting and contributing noise current that is directly referred to the input. Figure (10) shows the phase response of transimpedance amplifier. Figure (11) (a), (b) and (c) illustrate the simulation results of eye diagrams at 2.5, 5

and 7 Gb/s, respectively. The data jitter is about 0 ps for 2.5 Gb/s, 2 ps (peak to peak) for 5 Gb/s and 8 ps (peak to peak) for 7 Gb/s.

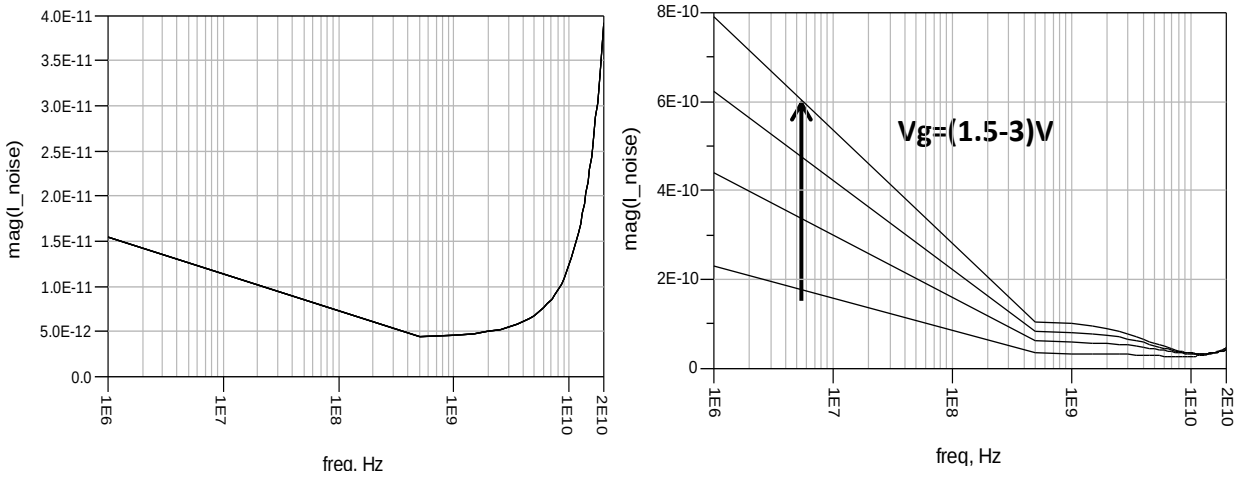


Fig. (9) Input referred noise of trans impedance amplifier (a) without variable gain (b) with variable gain (Vg is varied from 1.5V to 3v)

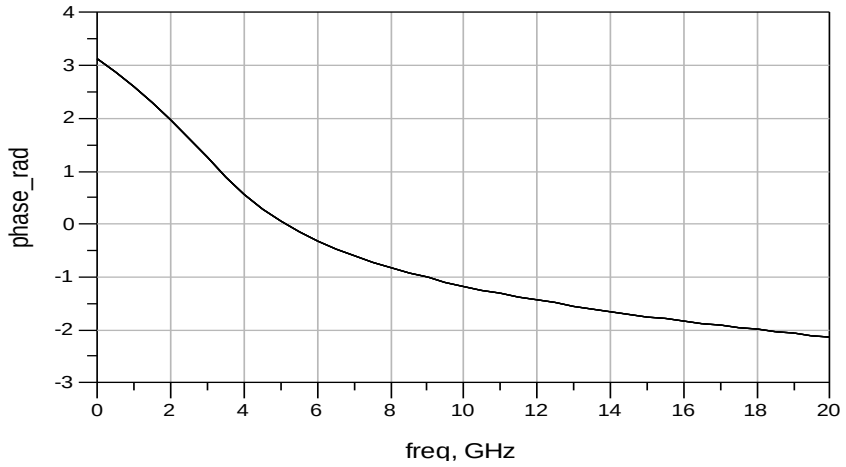
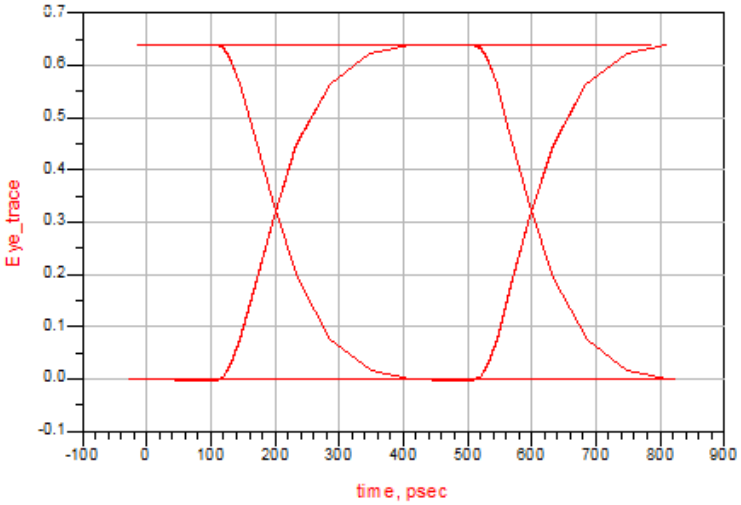
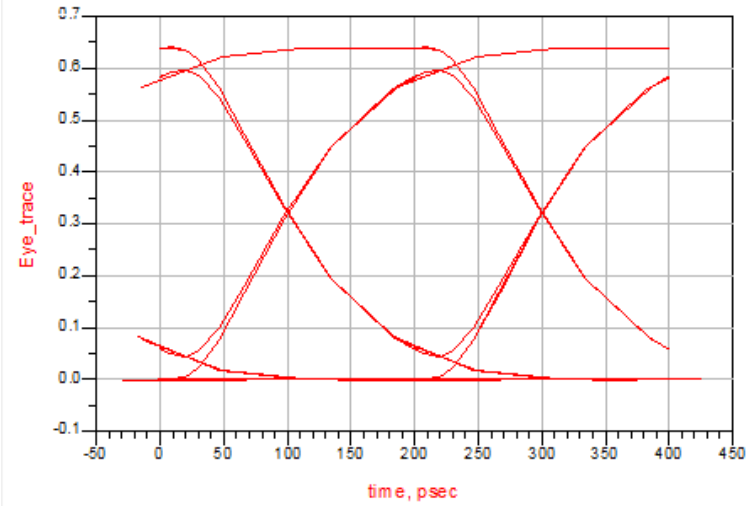


Figure (10) phase response of transimpedance amplifier



(a)



(b)

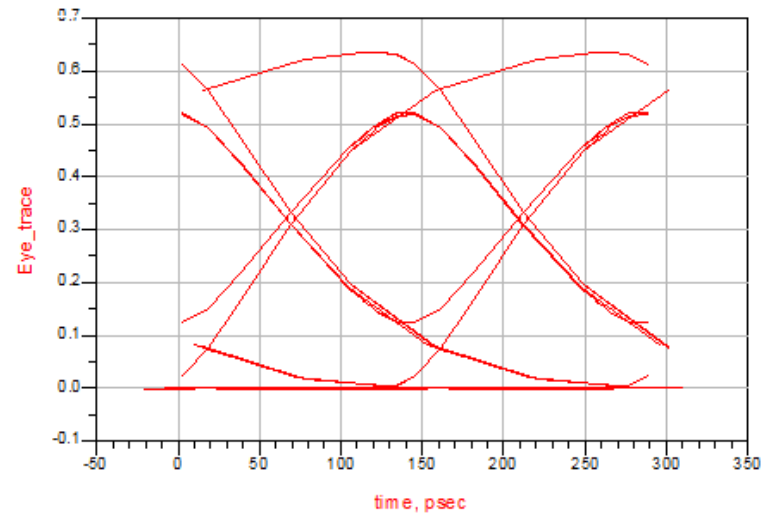


Figure (11) Eye diagrams of trans impedance amplifier for different data rates
(a) 2.5 Gb/s (b) 5 Gb (c) 7 Gb/s

Table (1) shows the performance comparison 5Gb/s trans impedance amplifier in this paper with some papers in the same data rate, Where obtained in this work the gain higher than found in the [7], [8], and [9] references, and the noise in this paper less from the [8] reference.

Power dissipation	Input Referred Nois	d.c gain (dBΩ)	Supply voltage (V)	CMOS technology	Ref.
24mW	–	66	1.8	0.18 μm	7
47mW	$13pA/\sqrt[2]{HZ}$	58.7	1.8	0.18 μm	8
29.66mW	–	55.75	1.8	0.18 μm	9
43.4mW	$5pA/\sqrt[2]{HZ}$	73	3.5	0.18 μm	This work

Conclusions:

The differential TIA designed based on 0.18 µm CMOS technology using RF large-signal model BSIM model in simulation , a maximum trans impedance gain of 73 dBΩ , trans impedance bandwidth of 3.1 GHZ and data rate 5Gb/s were obtained. The average input referred noise current spectral density over the TIA bandwidth is 5 pA / √Hz . The TIA also has a variable gain to increase the flexibility of the amplifier.

References

[1] Chin-Wei Kuo , Chao-Chih Hsiao , Shih-Cheng Yang and Yi-Jen Chan " The Design of CMOS Transimpedance Amplifier Based on BSIM Large-signal Model ", National Central University, pp. 165-168 , Chungli, Taiwan, 2004.
[2] Z. G. Wang, J. H. Lu, R. Tao, Z. Gu, X. H Chen, and L. Tina, " CMOS ICs Design for Gb/s Optic-Fiber Transmission Systems " , Institute of RF- & OE-ICs, pp. 5-8 , Nanjing, China , 2000 .
[3] Roger Yubtzuan Chen, Chih-Yuan Hung, and Tsung-Shuen Hung , " A CMOS Infrared Optical Preamplifier with a variable-gain transimpedance amplifier " , IEEE Asia-Pacific Conference , pp. 265-268 , Taiwan , 2004 .
[4] Mengxiong Li, " 5 Ghz Optical Front End In 0:35mm CMOS ", Ph.D. Thesis, University Of Nottingham, British, Oct. 2007.
[5] B. Razavi," Design of Integrated Circuits for Optical Communications ", McGraw- Hill, 2003.
[6] Rui Tao , Manfred Berroth , " A 10 Gb/s Fully Differential CMOS Transimpedance Preamplifier " , University of Stuttgart , pp. 1-4 , Germany , 2003 .
[7] B.Shammugasamy, T.Z. A. Zulkifli, and H. Ramiah, " A 24mW 5Gb/s fully balanced differential output trans-impedance amplifier with active inductor and capacitive degeneration techniques in 0.18μm CMOS technology " , IEICE Electronics Express, Vol.7, pp. 308-313, 2010.
[8] F. Beaudoin, M.N. El-Gamal, " A 5-Gbit/s CMOS optical receiver frontend " , IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2002), Vol. 3, pp. 168 - 171, 2002.
[9] Q. Feiyan, L. Lei, A. Qi1, and W. Yunfeng , " CMOS Preamplifier for High Performance Computing " , Proceedings of the 2009 International Workshop on Information Security and Application (IWISA 2009), pp. 425-428, Qingdao, China, November 21-22, 2009.

The work was carried out at the college of Engineering. University of Mosul